UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,581	12/12/2003	Satoru Konishi	H-1125	8605

7590 12/15/2005

Mattingly, Stanger & Malur, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/733,581	KONISHI ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-34* is/are allowed.

6)☒ Claim(s) *1,5,13,19-22,37 and 38* is/are rejected.

7)☒ Claim(s) *2-4,6-12,14-18,23,24,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203//12 Dec 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Hofstee et al. (US 2002/0074668 A1)

Nishizawa et al. (US 2001/0011766 A1)

Patel et al. (US 6,900,991 B2)

Park et al. (US 6,642,610 B2)

Farooq et al. (US 6,178,082 B1)

Jacobs et al. (US 4,811,082)

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al.

As to Claim 5, Nishizawa et al. discloses: a module board 1 having wiring 36, 38, 39 over an upper surface thereof and external electrode terminals 3a-g over a lower surface thereof; a first semiconductor chip 34b and a second semiconductor chip 34a formed over the module board 1 (Fig. 6) and including active elements (Fig. 5); and an integrated passive device 11a,b,c,d,e (a varistor; Figs. 4 and 5), wherein the first semiconductor chip 34b is mounted over the second semiconductor chip 34a (Figs. 5 and 6).

4. Claims 13 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Jacobs et al.

As to Claim 13, Jacobs et al. discloses, in Figs. 1 and 2: a module board 9 having wiring over an upper surface thereof and external electrode terminals over a lower surface thereof (Fig. 2; col.5: 47-51); a first semiconductor chip 32 and a second semiconductor chip 32 over which active elements are formed (col.5: 66-col.6: 3; and a first integrated passive device (thin film capacitors 13 integrated among the power layers 11; Fig. 2 and col.11: 45-col.12: 3), wherein the first semiconductor chip 32 and the second semiconductor chip are arranged at an upper surface side of module board 9 with a predetermined distance therebetween (Figs. 1 and 2).

As to Claim 19, Jacobs et al. further discloses that the first integrated passive device is arranged below the first semiconductor chip 32 (i.e., arranged within the layers 11 of module board 9; Fig. 2 and col.11: 45-58).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al. in view of Patel et al.

I. Farooq et al. discloses, in Fig. 1: a module board 11 having wiring over an upper surface thereof; a first semiconductor chip 15 and a second semiconductor chip (the other chip 15 shown in Fig. 1 or yet another semiconductor chip on the electronic component 10, as taught in col.1: 49-52) formed over module board 11 and including active elements; an integrated passive device 13 (Figs 1 and 2; col.4: 14-23); wherein one semiconductor chip out of the first and second semiconductor chips 15 and the integrated passive device 13 are mounted over an upper an upper surface of module board 11 in an overlapped manner (Fig. 1).

II. Farooq et al. does not depict the entire module board 11, and therefore does not depict the lower surface of module board 11. Accordingly, Farooq et al. is silent as to the claim limitation that the module board 11 has external electrode terminals over a lower surface thereof.

III. Patel et al. discloses, in Fig. 9, a module board 301 having wiring over an upper surface, a semiconductor chip 322 and an integrated passive device (capacitor) 310, wherein the chip 322 and integrated passive device 310 are overlapped. Patel et

al. further discloses that the lower surface of module board 301 has external electrode terminals over a surface thereof for mounting the module board to a system PCB 330.

IV. Since Farooq et al. and Patel et al. are both in the same art of electronic packaging, then providing external electrode terminals over a lower surface of the module for the purpose of mounting the resultant package to a PCB as part of an electronic system, as taught by Patel et al., would have been readily recognized as an application for the package disclosed in the pertinent art of Farooq et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide external electrode terminals over a lower surface of the module board of Farooq et al. in order to enable a mounting of the module board package to a system PCB for an electronic application, as taught in Patel et al.

8. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al., as applied to Claim 1 above, and further in view of Hofstee et al.

As to Claims 37 and 38:

I. Farooq et al., as modified by Patel et al., does not teach that the first chip, second chip and integrated passive device are covered with a sealing portion made of insulating resin, and does not teach that end portions of the sealing portion are not positioned outside the end portions of the module board.

II. Hofstee et al. discloses, in Fig. 2, a stacked chip assembly mounted on the upper surface wiring of a module board and covered with a sealing portion made of insulating resin (plastic) 202 (p.2, lines 3-9 of paragraph [0016]) for the purpose of

protecting the chips from environmental contaminants and mechanical forces, wherein the end portions of the insulating resin 202 are not positioned outside the end portions of the module board, effectively keeping the package size as small as possible.

III. Since modified Farooq et al. and Hofstee et al. disclose stacked chip assemblies on a module board, then the protection of the chip assembly by applying an insulating resin as compactly as possible (i.e., limiting the resin application to no further than the dimensions of the module board perimeter) would have been readily recognized as an effective protection for the package that also ensures the miniaturization desired for the electronic system application.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Farooq et al. by covering the chips 15, capacitors 13 and other devices on the module board 11 of Farooq et al. with the insulating resin used as a sealing portion of the package, and applying the resin such that the end portions of the resin sealing portion are not positioned outside the end portions of the module board in order to protect the chips without increasing the x-y dimensions of the module board.

9. Claims 13, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al. in view of Patel et al.

As to Claim 13:

I. Farooq et al. discloses, in Fig. 1: a module board 11 having wiring over an upper surface thereof; a first semiconductor chip 15 and a second semiconductor chip 15 over which active elements are formed (col.1: 49-52); and a first integrated passive

device 13 (Figs. 1 and 2; col.4: 14-23), wherein the first semiconductor chip 15 and the second semiconductor chip 15 are arranged at an upper surface side of the module board with a predetermined distance therebetween (Fig. 1).

II. Farooq et al. does not depict the entire module board 11, and therefore does not depict the lower surface of module board 11. Accordingly, Farooq et al. is silent as to the claim limitation that the module board 11 has external electrode terminals over a lower surface thereof.

III. Patel et al. discloses, in Fig. 9, a module board 301 having wiring over an upper surface, a semiconductor chip 322 and an integrated passive device (capacitor) 310, wherein the chip 322 and integrated passive device 310 are overlapped. Patel et al. further discloses that the lower surface of module board 301 has external electrode terminals over a surface thereof for mounting the module board to a system PCB 330.

IV. Since Farooq et al. and Patel et al. are both in the same art of electronic packaging, then providing external electrode terminals over a lower surface of the module for the purpose of mounting the resultant package to a PCB as part of an electronic system, as taught by Patel et al., would have been readily recognized as an application for the package disclosed in the pertinent art of Farooq et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide external electrode terminals over a lower surface of the module board of Farooq et al. in order to enable a mounting of the module board package to a system PCB for an electronic application, as taught in Patel et al.

As to Claim 19, modified Farooq et al. further discloses the first integrated passive device 13 is arranged below the first semiconductor chip 15 (Fig. 1).

As to Claim 20, modified Farooq et al. further discloses the first integrated passive device 13 is mounted over the upper surface of the module board 11 by flip-chip connection (Fig. 1; col.3: 46-49).

10. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al. in view of Patel et al., as applied to Claims 19 and 20 above, and further in view of Park et al.

As to Claims 21 and 22:

I. Modified Farooq et al. discloses the module board 11 may have other devices besides semiconductor chips 15 mounted thereon, such as microprocessors, SRAMs, DRAMs and chips (col.3: 49-52) but does not explicitly teach discrete parts mounted over the upper surface of the module board.

II. Park et al. discloses, in Fig. 7, a multichip module that includes discrete parts including surface mount resistors and inductors on the upper surface of the module board for performing current limiting, signal conditioning, etc. for the semiconductor chip components (col.9: 65-col.10: 2).

III. Since modified Farooq et al. discloses semiconductor chips 15 and capacitors 13 already in stacked assembly, and further teaches that other semiconductor devices may be mounted thereon in addition to semiconductor chips 15, then the use of discrete parts such as surface mount resistors and inductors, and even additional surface mount capacitors in the electronic system circuit, as taught by Park et al., would have been

readily recognized as useful, even necessary, for current limiting and signal conditioning in the pertinent art of Farooq et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Farooq et al. by including surface mount resistors, inductors, and even capacitors, on the upper surface of the module board, as taught by Park et al., on the upper surface of the module 11, in addition to the stacked chip/capacitor structures, microprocessors, memory chips, etc. of Farooq et al., in order to perform the necessary current limiting and signal conditioning functions required by the above-cited semiconductor devices in the electronic application of Farooq et al., as taught by Park et al.

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. in view of Park et al.

I. Jacobs et al. discloses all the limitations of Claim 19, including a multichip module board 9 having semiconductor chips 32 mounted over the upper surface thereof, but does not teach additional discrete parts mounted over the upper surface thereof.

II. Park et al. discloses, in Fig. 7, a multichip module that includes discrete parts including surface mount resistors and inductors on the upper surface of the module board for performing current limiting, signal conditioning, etc. for the semiconductor chip components (col.9: 65-col.10: 2).

III. Since Jacobs et al. discloses semiconductor chips 32 in a multichip module, as does Park et al., then the use of discrete parts such as surface mount resistors,

inductors and capacitors for the purpose of current limiting and signal conditioning (e.g., filtering, impedance matching and control, etc.), as taught by Park et al., would have been readily recognized for use in the multichip module 9 as applied to the electronic system of Fig. 1 of Jacobs et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include surface mount resistors, inductors and/or capacitors on the upper surface of the module board, as taught by Park et al., in order to perform the necessary current limiting and signal conditioning functions required by the semiconductor chips for optimizing their functions in the electronic system of Jacobs et al.

Allowable Subject Matter

12. Claims 25-29, 30-32 and 33-34 have been allowed.

13. Claims 2-4, 6-12, 14-18, 23-24 and 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

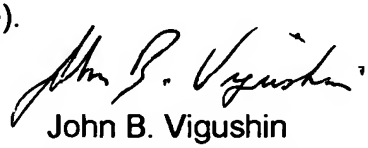
14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Moresco (US 6,535,398 B1) discloses integrated passive devices positioned under respective semiconductor chips 4 (col.3: 65-col.4: 6; col.4: 58-63).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 10, 2005